IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: CHANG, Yi-Yang

SERIAL NO.:

FILED: Herewith

TITLE: SIGNAL DETECTOR

Preliminary Amendment: CLAIM AMENDMENTS

1. (Currently amended) A clock signal detector which is designed to be used in telecommunication transmission systems~~. This~~, said clock signal detector ~~contains:~~ comprising:

a signal converter, which converts coupled input differential clock signal into single output clock signal~~.~~;

a rectifying-filtering circuit~~, which is~~ connected to the signal converter and ~~converts~~ converting clock signals outputted from the signal converter into DC potential signal output~~.~~; and

an inverter ~~which is~~ connected to the rectifying-filtering circuit and ~~outputs~~ outputting the D.C. potential signal from the rectifying-filtering circuit as a reversed potential signal~~.~~

~~In summary, the clock signal detector detects~~; wherein interruptions in clock signal transmission~~.~~ ~~When~~ are detected such that when the interruption occurs, the signal converter and rectifying-filtering circuit cease to correspondingly output clock signal and D.C. potential signal~~.~~ ~~Once~~; and wherein, once this is detected, the inverter outputs a high-potential signal, that is, a clock signal transmission abnormality detection potential signal.

2. (Original) The clock signal detector as defined in claim 1, wherein said the signal converter serves to convert Low-Voltage Positive Emitter Coupling Logic (LVPECL) signal (input end) into Low-Voltage Transistor-Transistor Logic (LVTTL) signal (output end).

3. (Currently amended) The clock signal detector as defined in claim 1, wherein said ~~the~~ rectifying-filtering circuit ~~can be~~ is comprised of a stand-alone rectifying component (i.e. micro inductor)

4. (Currently amended) The clock signal detector as defined in claim 1, wherein said ~~the~~ inverter ~~can be an~~ is comprised of a transistor circuit~~. At the~~, at an input end, the regularly present D.C. potential signal ~~is~~ being inputted into the base of the transistor, which connects the circuit between the collector and emitter of the transistor~~;~~ and~~;~~ regularly outputs a low potential from the output end at the collector~~. Conversely,~~; and wherein, when the clock signal disappears, the circuit closes the conduction between the collector and emitter of the transistor to trigger a high-potential output from the output end at the collector of the transistor~~. This mechanism achieves~~; and wherein the effect of inversion is achieved, and the signal outputted is the so-called clock signal transmission abnormality detection potential signal.

5. (Currently amended) The clock signal detector as defined in claim 1, wherein said ~~the~~ output end can be connected to an interruption control circuit at the emission end of a transmission system (i.e. laser emitter of the fiber-optic transmitter)~~. The~~; and wherein a potential signal of clock

signal transmission abnormality detection is used to drive the interruption control circuit to stop the signals from being continuously emitted.

6. (Currently amended) A data signal detector which is designed to be used in telecommunication transmission systems. ~~This~~ said data signal detector ~~contains:~~ comprising:

a signal converter~~, which converts~~ converting coupled input differential data signal into single output data signal~~:~~;

an Integral Charger~~, which is~~ connected to the signal converter and ~~converts~~ converting the data signal inputted from the signal converter into a pulse type integral potential signal output. ~~This~~, wherein the potential signal approximately corresponds to a constant ratio of positive potential signal pulse~~:~~; and

an inverter~~, which is~~ connected to the integral charger and ~~outputs~~ outputting a D.C. potential signal from the integral charger as a reversed potential signal~~:~~

~~———~~; wherein the data signal detector is capable of detecting overly high data ratio of data signals~~:~~ ~~When~~; and wherein, when the data ratio of positive potential signal in the differential data signal transmission becomes overly high, the signal converter and integral charger correspondingly output a higher ratio data signal and integral potential signal, and when the output surpassed the defined potential level, the inverter outputs a low-potential signal, that is, the data signal transmission abnormality detection potential signal.

7. (Original) The data signal detector as defined in claim 6, the signal converter serves to convert Low-Voltage Positive Emitter Coupling Logic (LVPECL) signal (input end) into Low-Voltage Transistor-Transistor Logic (LVTTL) signal (output end).

8. (Currently amended) The data signal detector as defined in claim 6, the second resister of the integral charger can be connected to the capacitor in parallel, which is then connected to the first resister with a tandem connection~~. In which,~~; wherein the first resistor is the input end and the tandem connection point between the first resistor and the second resistor is the output end~~. The other~~ and another end of the second resistor is grounded~~. The~~; and wherein threshold voltage output potential is Vb and the charge formula is Vb = Va * VR * [1-e(-t/TC)] + Vinitial e raise the power of (-t/TC)~~. In~~ , in which,

TC = R1 * R2 * C2/(R1+R2)

VR = R2/(R1+R2)

Vinitial = Va * VR/2

9. (Currently amended) The data signal detector as defined in claim 6, this inverter serves as a Logic Gate and makes logic decisions to the inputted integral potential signal~~. It enables~~, enabling, while input of a constant ratio of integral potential pulses and reverses the potential pulses into a high potential signal for output~~. When~~, wherein the data ratio of positive potential signal in the differential data signal transmission becomes overly high, ~~it is~~ then being inputted as a higher ratio integral signal pulse and reversed into a low-potential signal for output~~. Through~~; and wherein this

mechanism, reversion is achieved, and the outputted signal is the so-called data signal transmission abnormality detection potential signal.

10. (Currently amended) The data signal detector as defined in claim 6, the output end can be connected to an interruption control circuit at the emission end of a transmission system (i.e. laser emitter of the fiber-optic transmitter end). ~~The~~, and wherein potential signal of data signal transmission abnormality detection is used to drive the interruption control circuit to stop the signals from being continuously emitted.

11. (Currently amended) ~~It is a type of~~ A signal detector, which is designed to be used in telecommunication transmission systems. ~~The~~, said signal detector ~~includes the following major components:~~ comprising:

a signal converter~~, which converts~~ converting coupled input differential data signal into single output data signal~~:~~;

a clock signal detector ~~which receives the above-mentioned~~ receiving converted single output clock signals~~. When~~; wherein, when this single output clock signal is in a normal state, the clock signal detector outputs a low-potential clock detection signal, and when this single output clock signal is interrupted, the system outputs a high-potential clock detection signal~~:~~;

a data signal detector~~, which receives the above-mentioned~~ receiving converted single output data signals~~. When~~; wherein, when this single output data signal is in a normal state, the data signal detector outputs a low-potential data detection signal, and when this single output data signal

is in an abnormal state and outputs positive potential continuously, the system outputs a high-potential data detection signal~~.~~

~~———————~~; and an interruption control circuit~~, which receives the above-mentioned~~ receiving converted clock and data signals and ~~determines the~~ determining production of control signals according to the potential states of the clock and data detection signals~~.~~

~~——— Through the above-stated~~; wherein, through the control signal, the interruption control circuit controls whether to emit transmission signals at the emission end of the transmission system.

12. (Currently amended) The signal detector as defined in claim 11, the ~~clock~~ signal detector ~~includes the following:~~ comprising:

a signal converter~~, which converts~~ converting coupled input differential clock signal into single output clock signal~~.~~;

a rectifying-filtering circuit~~, which is~~ connected to the signal converter and ~~converts~~ converting clock signals outputted from the signal converter into DC potential signal output~~.~~; and

an inverter~~, which is~~ connected to the rectifying-filtering circuit and ~~outputs~~ outputting a D.C. potential signal from the rectifying-filtering circuit as a reversed potential signal~~.~~

~~——— In summary, the~~; wherein the clock signal detector detects interruptions in clock signal transmission~~. When~~; wherein, when the interruption occurs, the signal converter and rectifying-filtering circuit cease to correspondingly output clock signal and D.C. potential signal~~. Once this is~~; and wherein, once detected, the inverter outputs a high-potential signal, that is, a clock signal transmission abnormality detection potential signal.

13. (Currently amended) The signal detector as defined in claim 11, ~~the data~~ wherein the signal detector ~~includes the following:~~ comprising:

a signal converter~~, which converts~~ converting coupled input differential data signal into single output data signal~~:~~;

an Integral Charger~~, which is~~ connected to the signal converter and ~~converts~~ converting the data signal inputted from the signal converter into a pulse type integral potential signal output~~. This~~; wherein the potential signal approximately corresponds to a constant ratio of positive potential signal pulse~~:~~; and

an inverter~~, which is~~ connected to the integral charger and ~~outputs~~ outputting a D.C. potential signal from the integral charger as a reversed potential signal~~:~~

~~———————~~ wherein the data signal detector is capable of detecting overly high data ratio of data signal~~. When~~; and wherein, when the data ratio of positive potential signal in the differential data signal transmission becomes overly high, the signal converter and integral charger correspondingly output a higher ratio data signal and integral potential signal, and when the output surpassed the defined potential level, the inverter outputs a low-potential signal, that is, the data signal transmission abnormality detection potential signal.

14. (Currently amended) The signal detector as defined in claim 11, the output end of the clock signal detector and data signal detector can be individually connected to the interruption control circuit at the emission ends of the transmission system (i.e. laser emitter of the fiber-optic transmitter)~~. The~~ and wherein the potential signal of data signal transmission abnormality detection,

in conjunction with the potential signal of clock signal abnormality detection, is used to drive the interruption control circuit to stop the signals from being continuously emitted.

15. (Original) The signal detector as defined in claim 11, the potential states of clock and data detection signals, as described in the interruption control circuit section, refer to the positive potential control signals used to interrupt signal emission from the emitting end of the transmission system when an interruption in clock signal or abnormal continuous transmission of data signal occur; contrariwise, the control signal will not be produced.

16. (Currently amended) The signal detector as defined in ~~claims 11 and 13,~~ Claim 11, wherein the second resister of the integral charger can be connected to the capacitor in parallel, which is then connected to the first resister with a tandem connection~~. In which,~~; wherein the first resistor is the input end and the tandem connection point between the first resistor and the second resistor is the output end~~. The other~~ , wherein another end of the second resistor is grounded~~. The~~, and wherein threshold voltage output potential is Vb and the charge formula is Vb = Va * VR * [1-e(-t/TC)] + Vinitial e raise the power of (-t/TC)~~. In~~ in which,

TC = R1 * R2 * C2/(R1+R2)

VR = R2/(R1+R2)

Vinitial = Va * VR/2